

FIG. 1

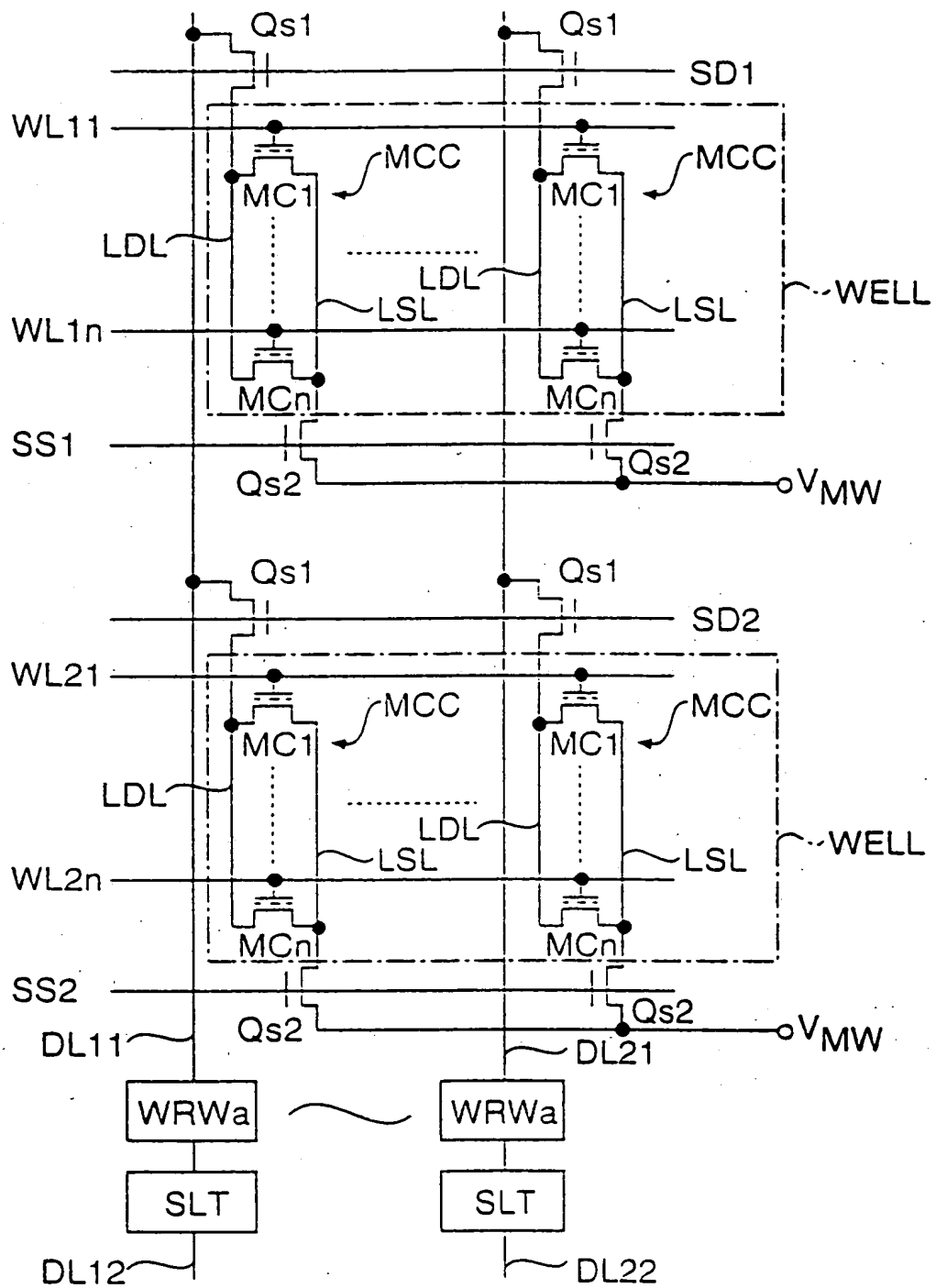
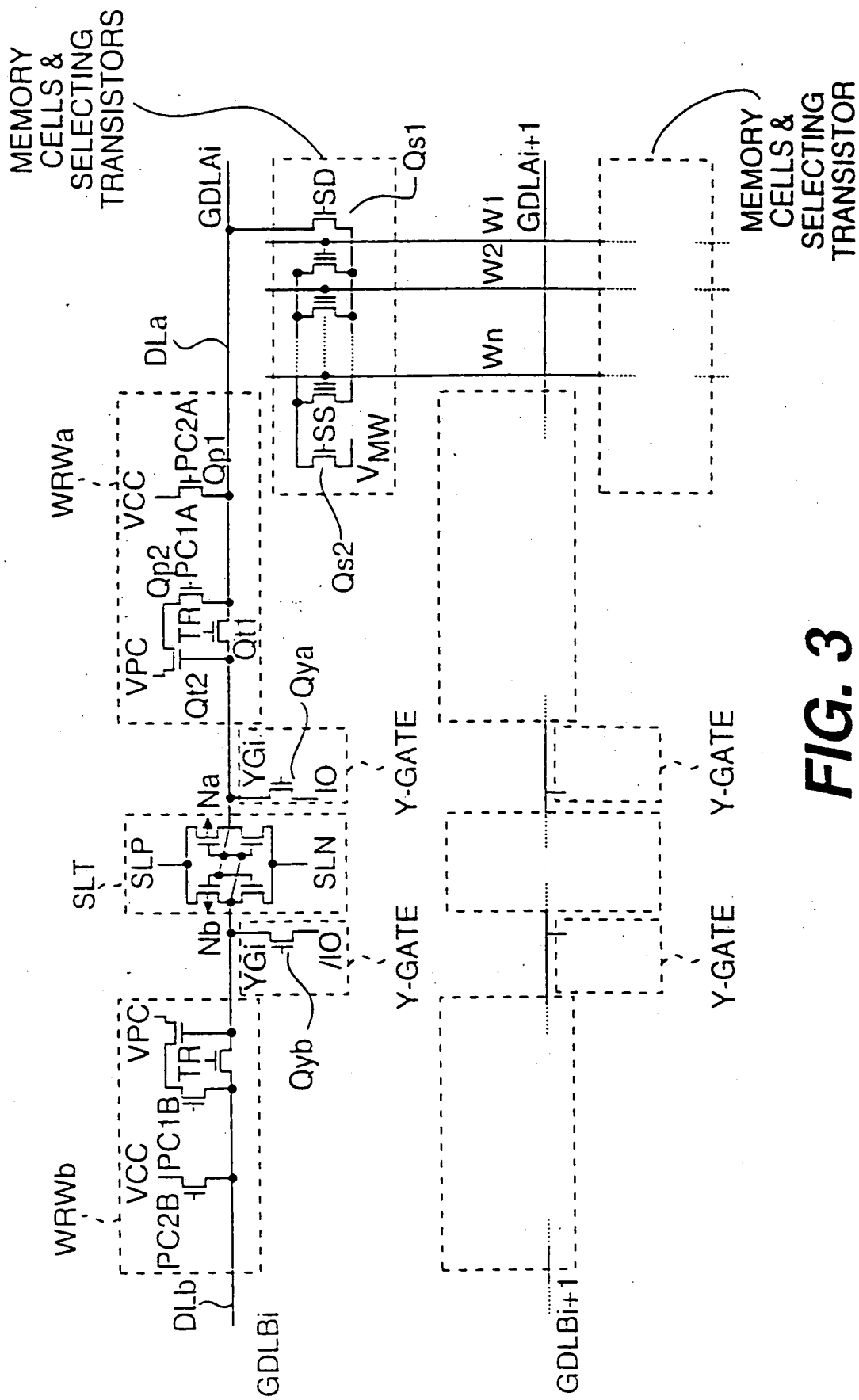


FIG. 2



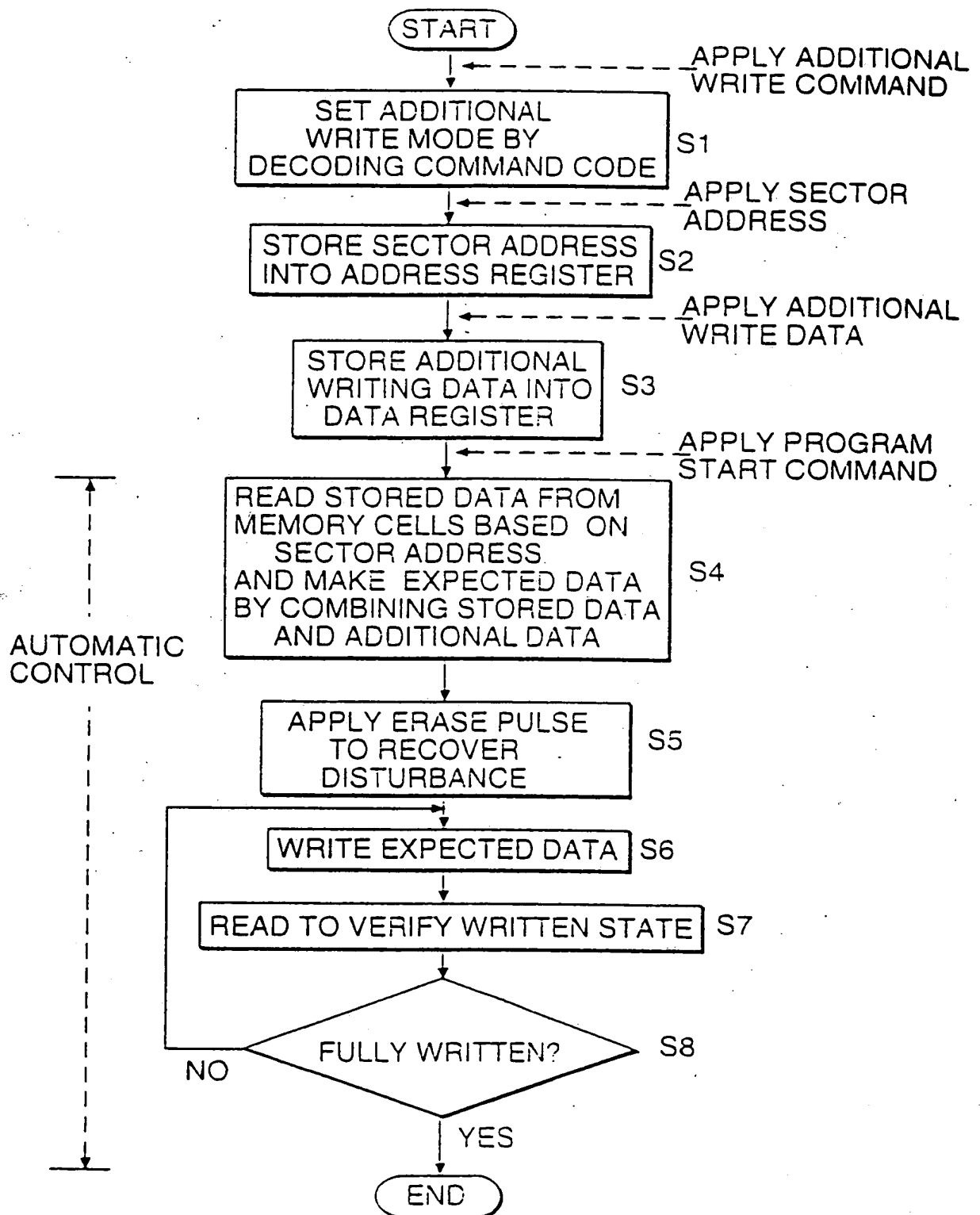


FIG. 4

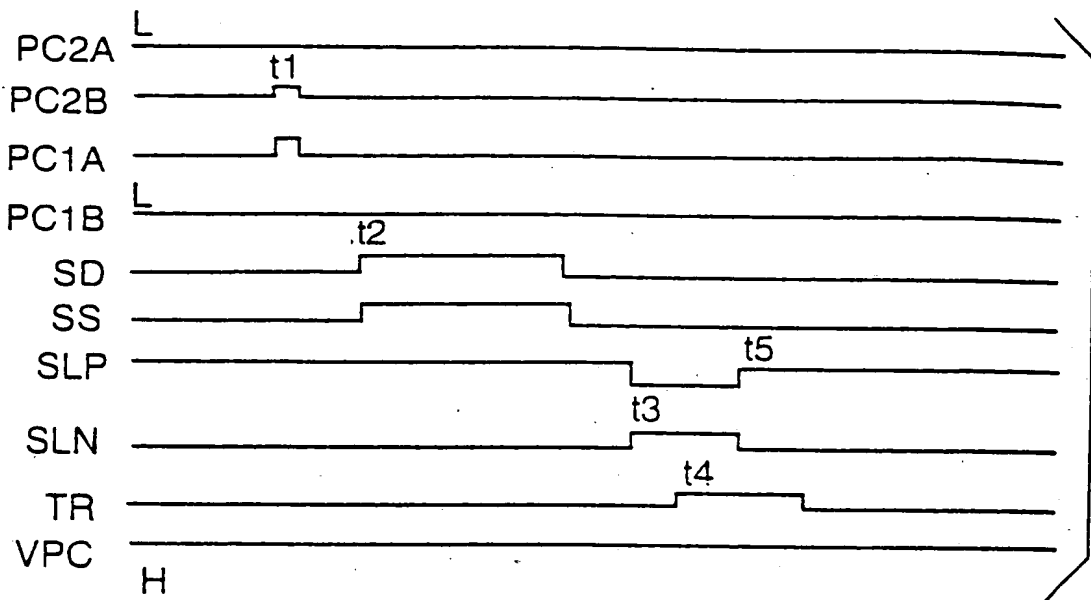


FIG. 5

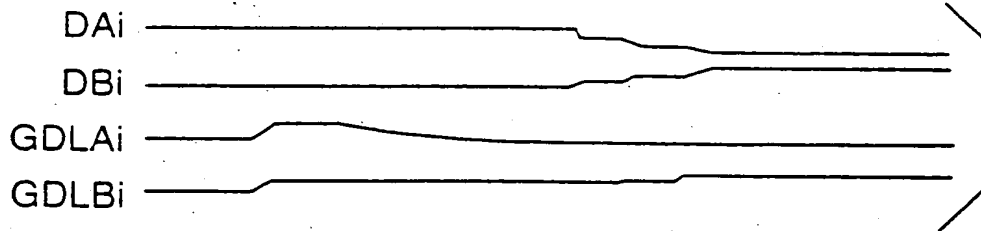


FIG. 6(a)

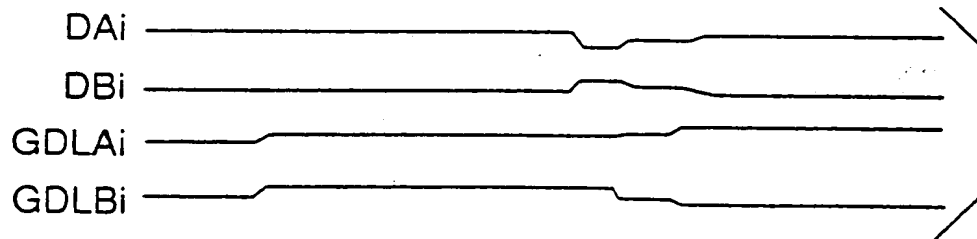


FIG. 6(b)

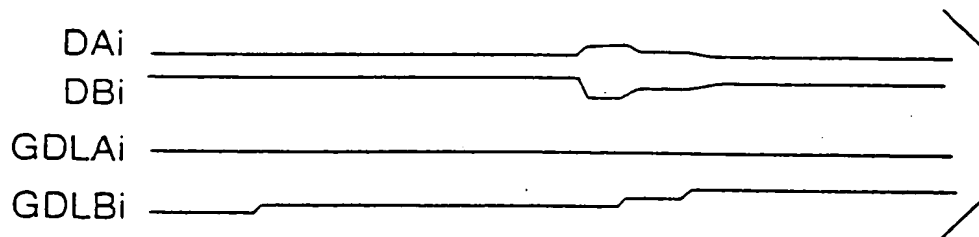


FIG. 6(c)

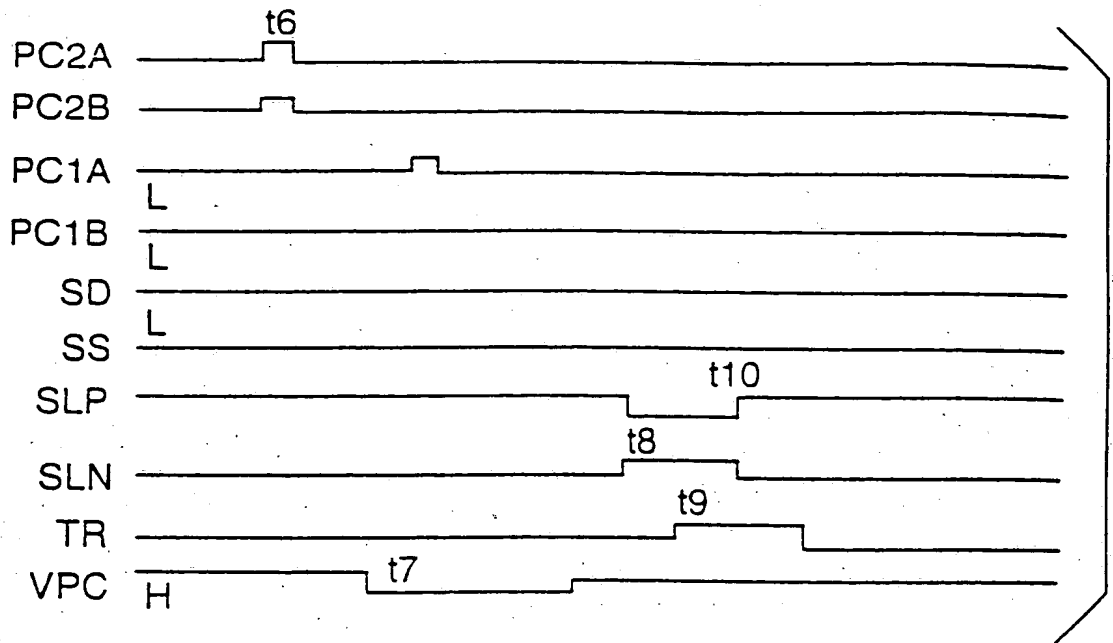


FIG. 7

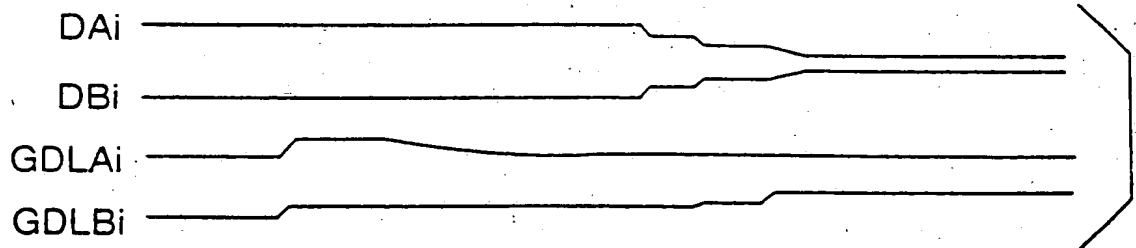


FIG. 8(a)

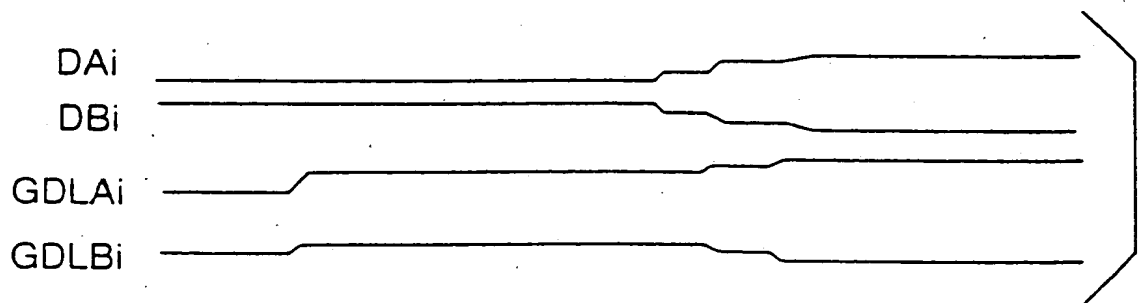


FIG. 8(b)

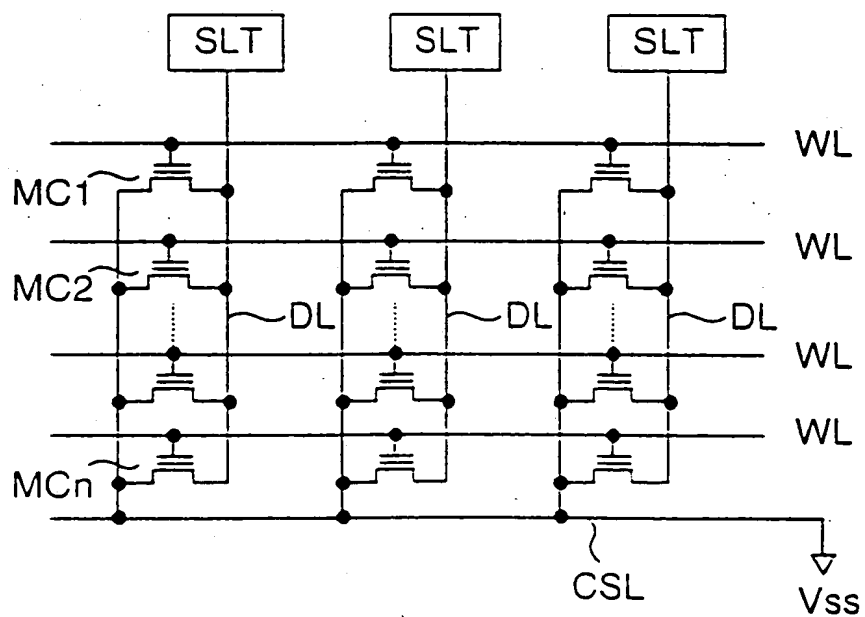
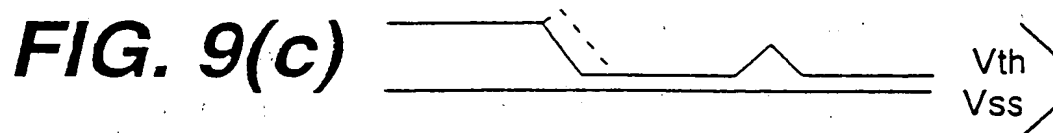
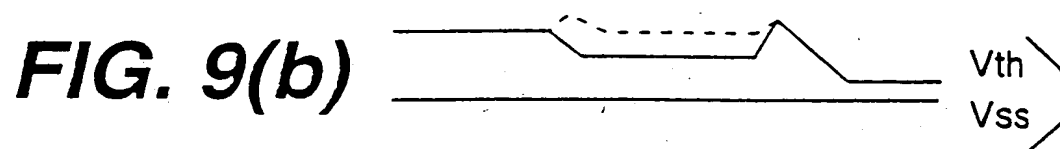
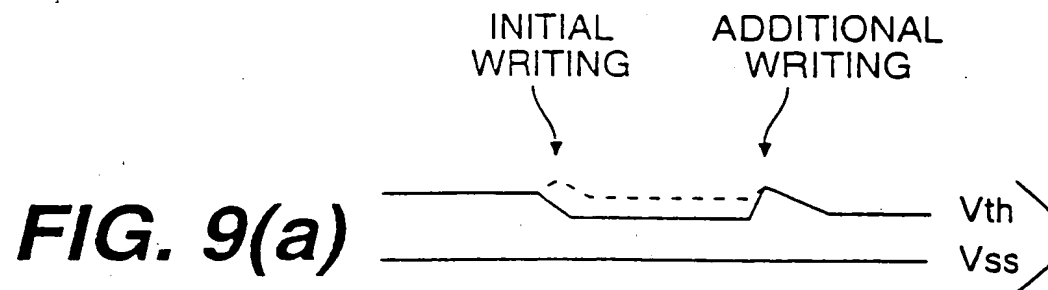
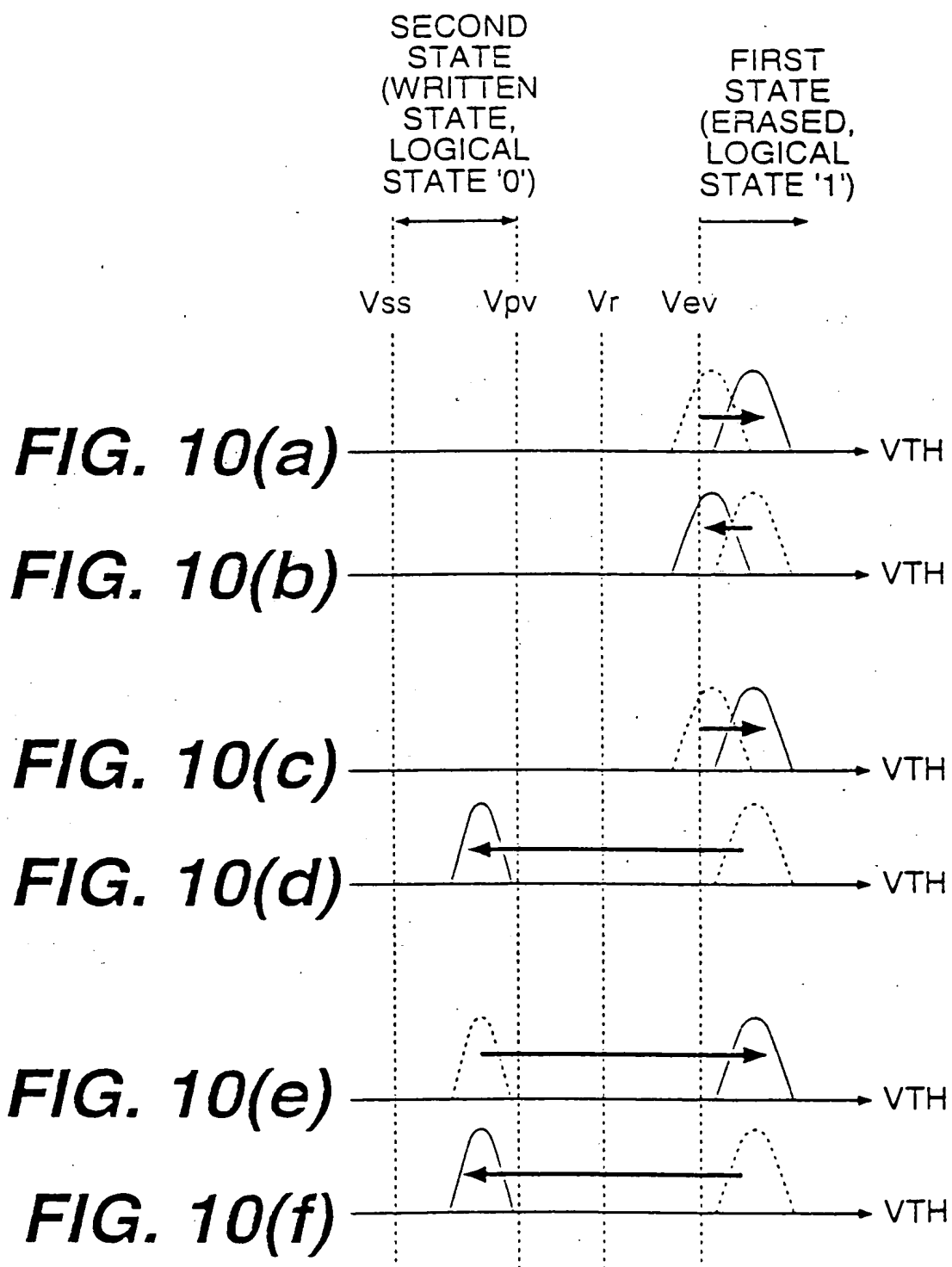
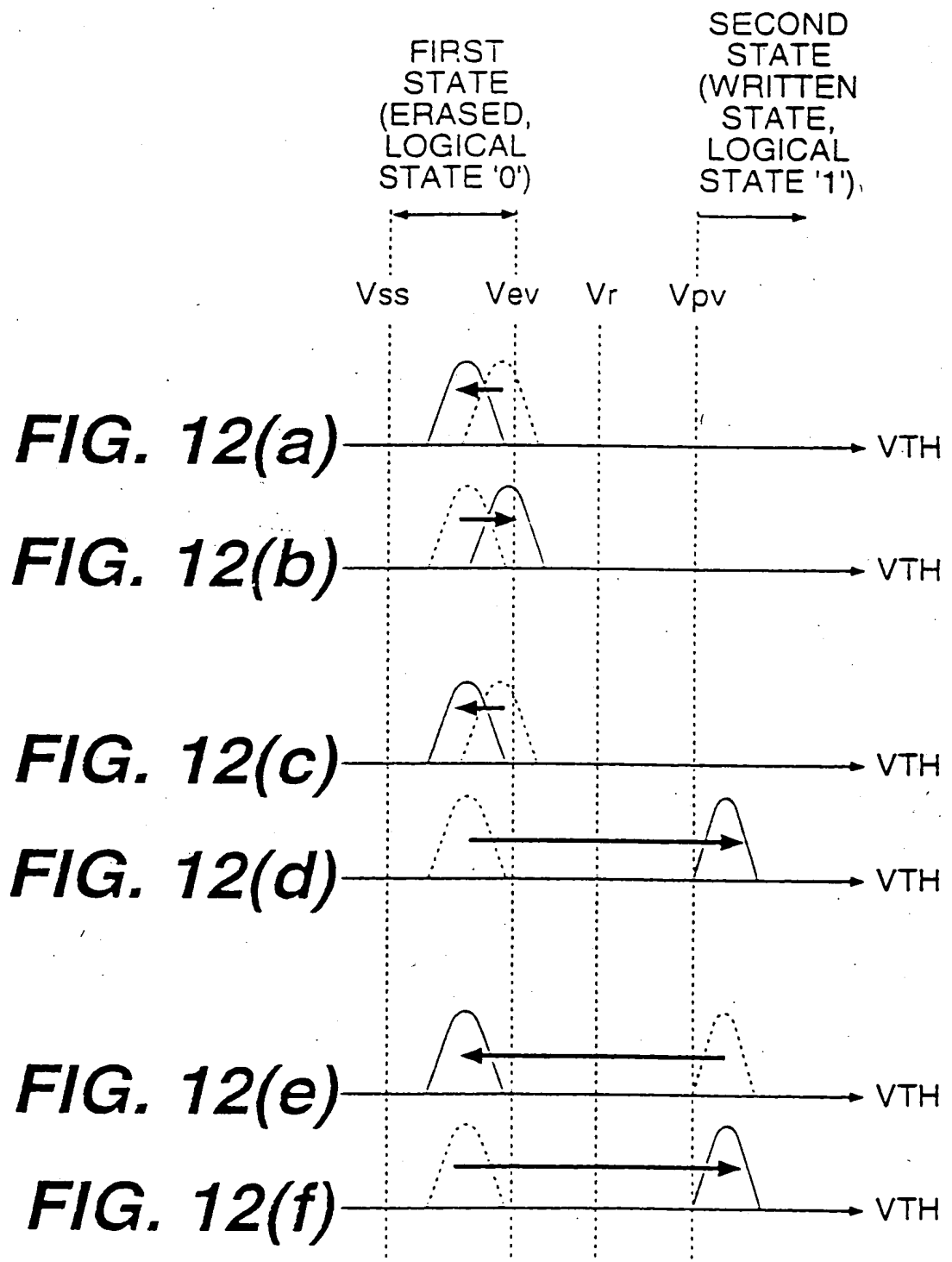


FIG. 11





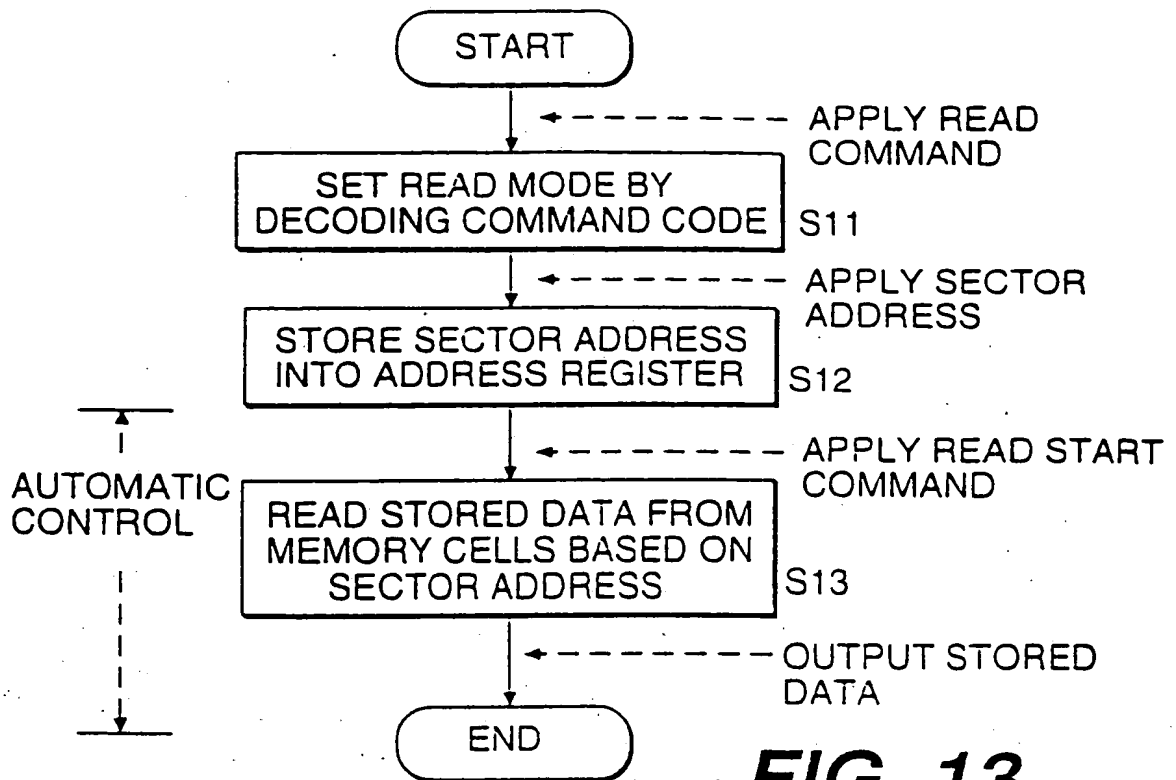


FIG. 13

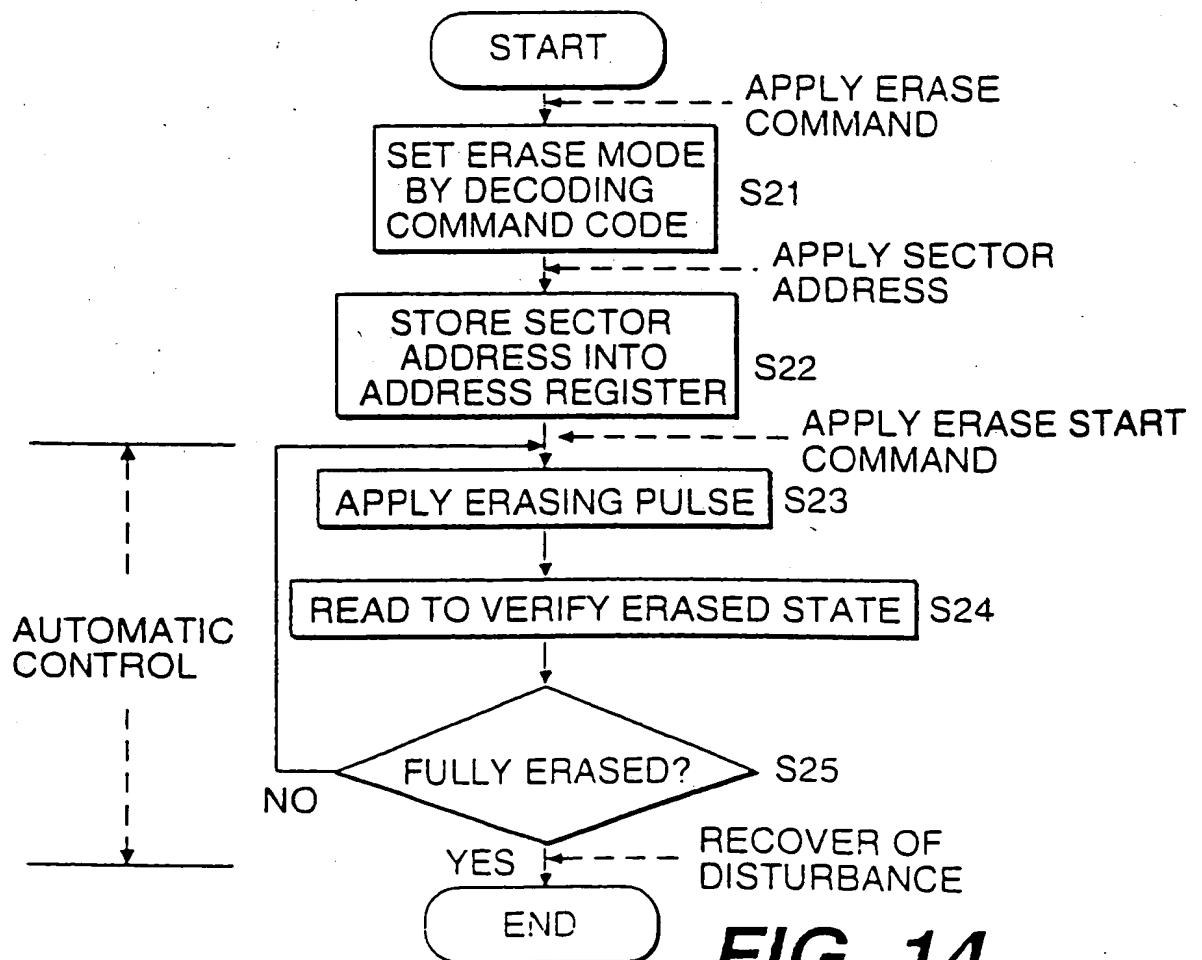


FIG. 14

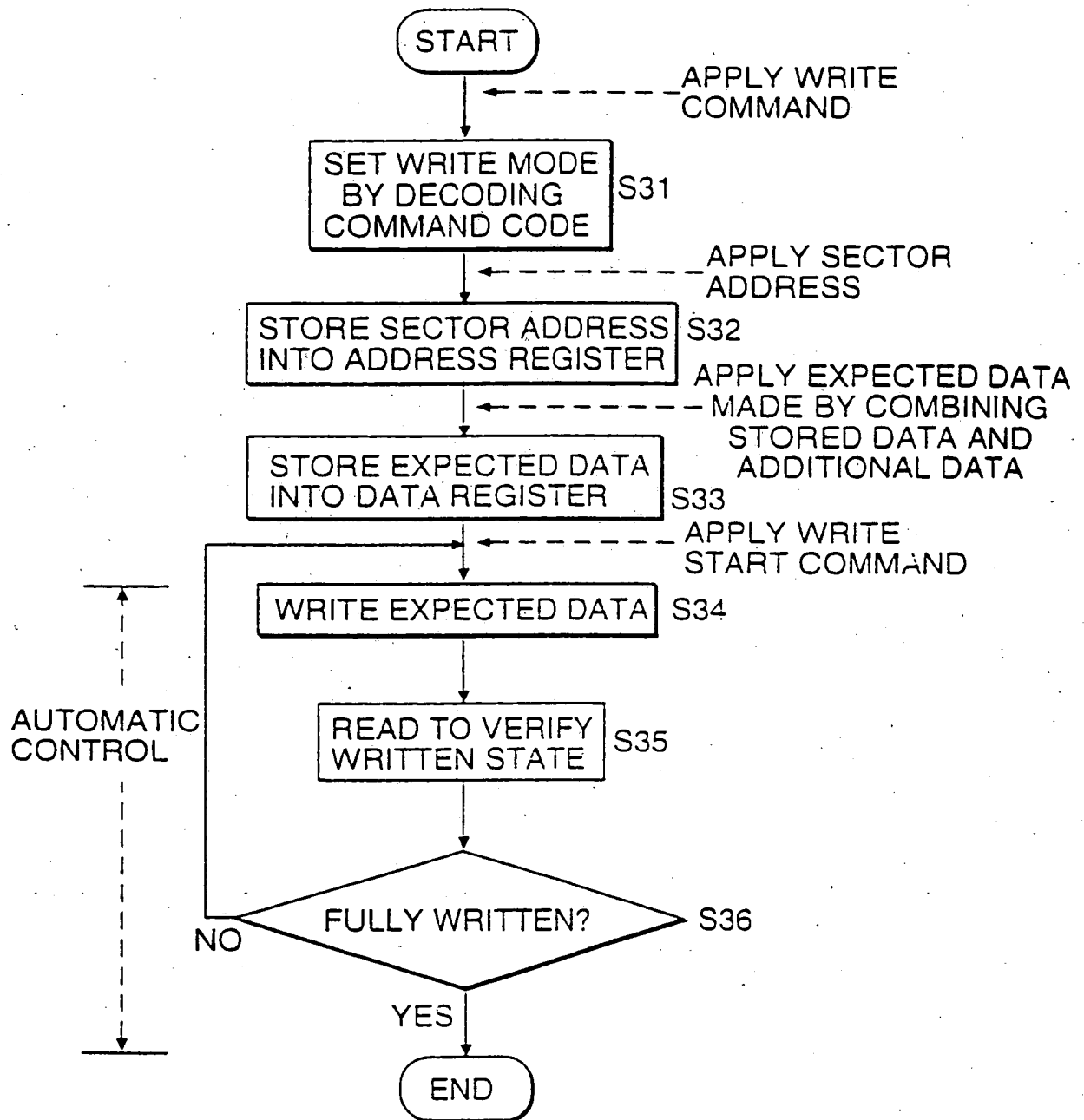


FIG. 15

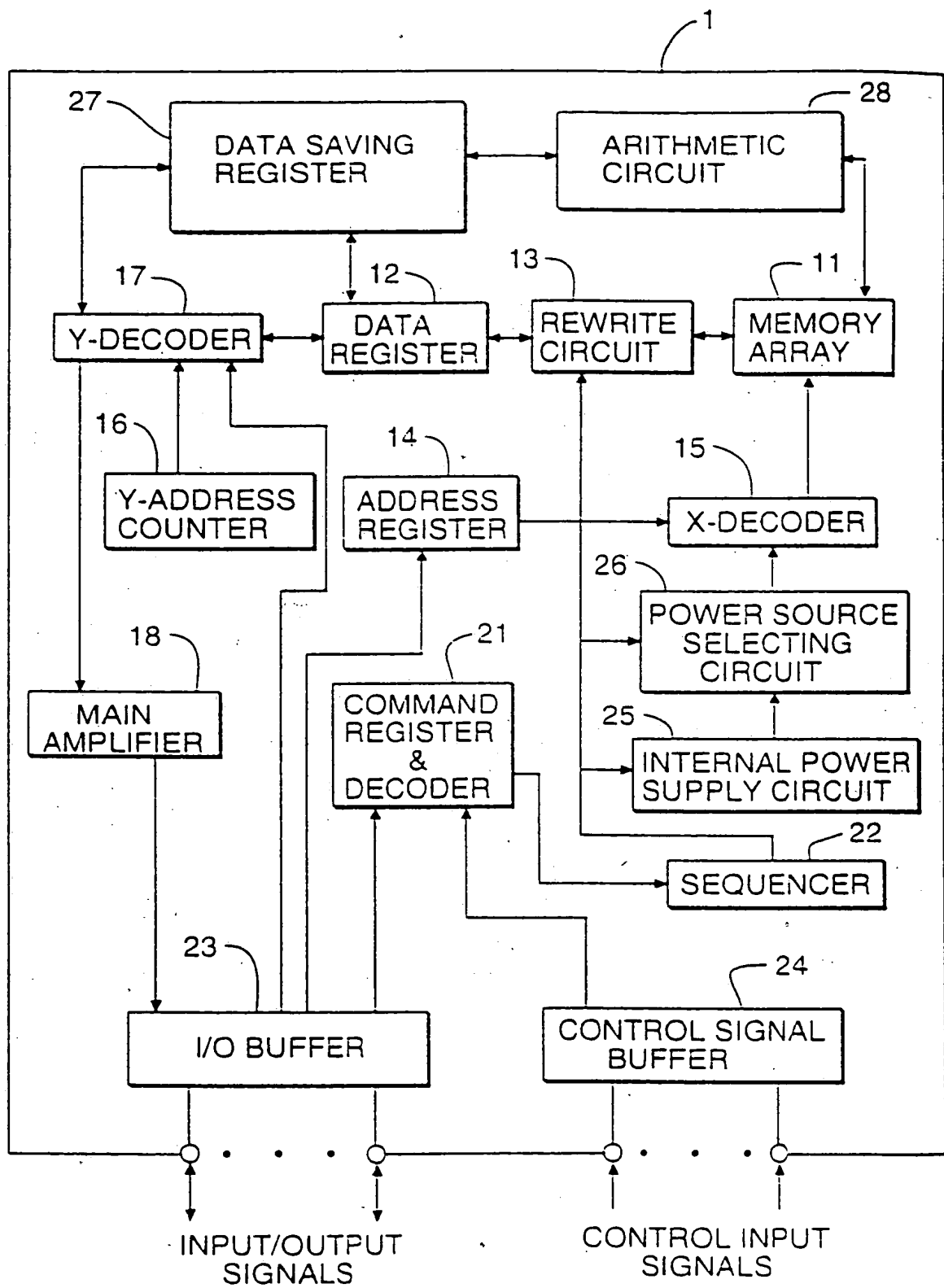


FIG. 16

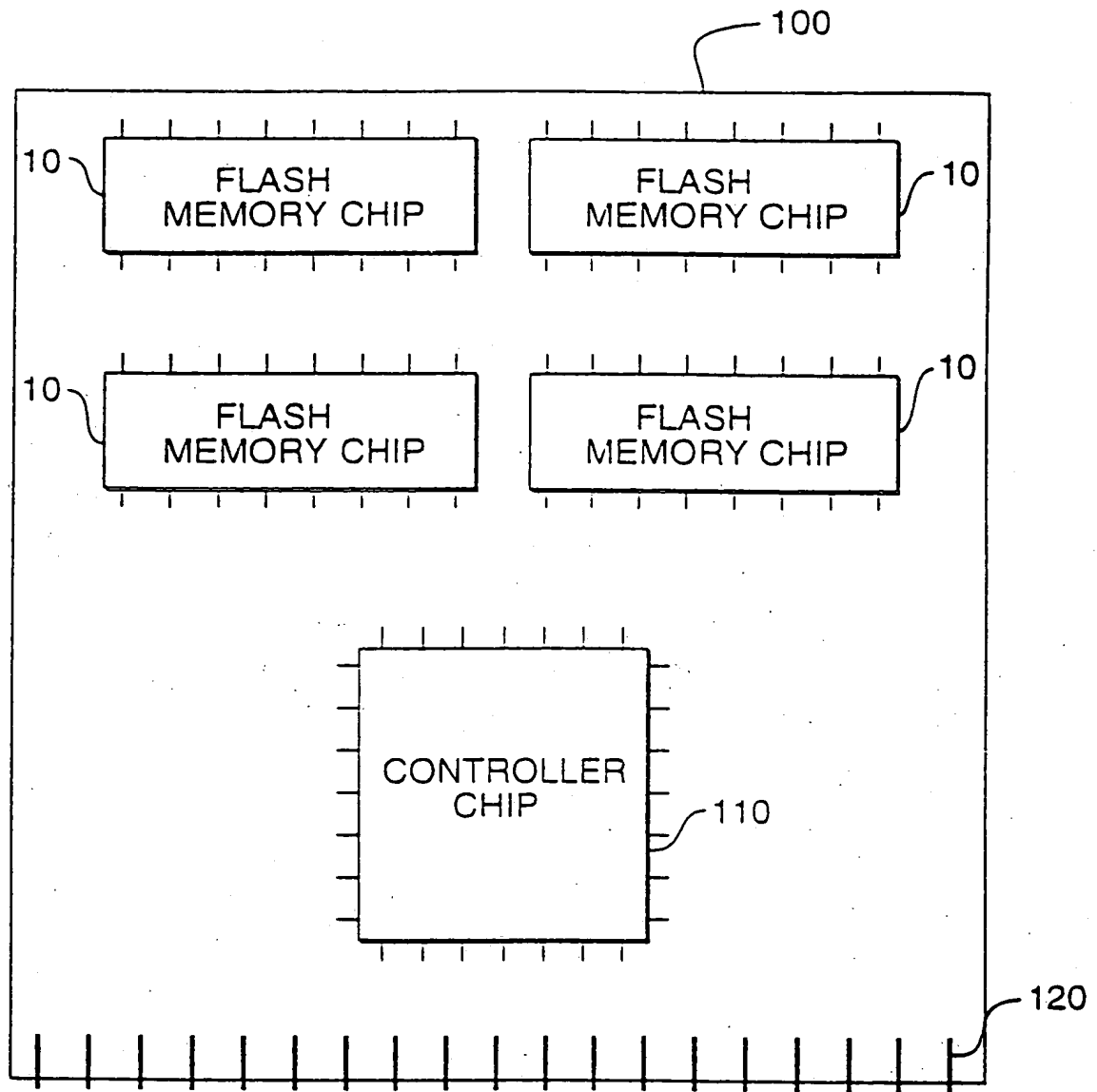


FIG. 17

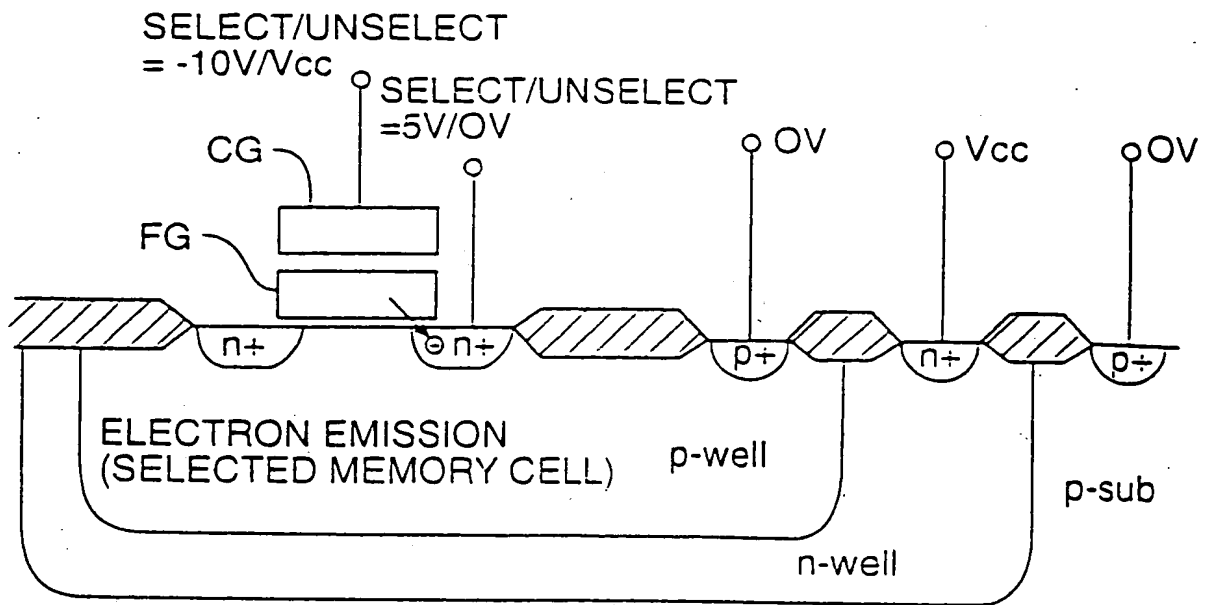


FIG. 18

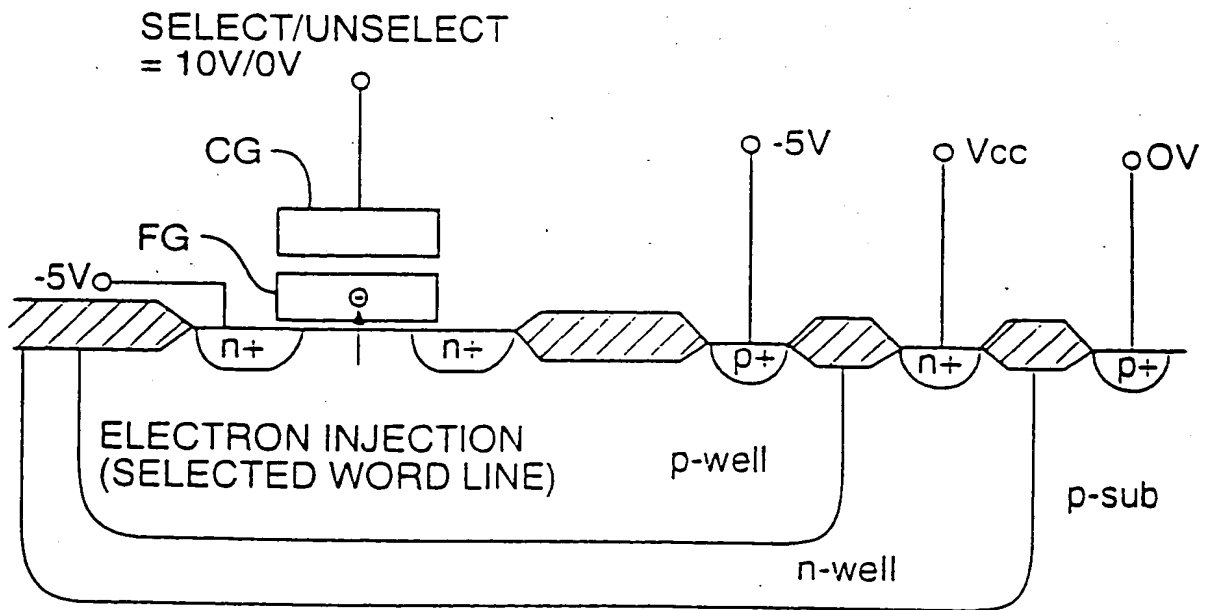
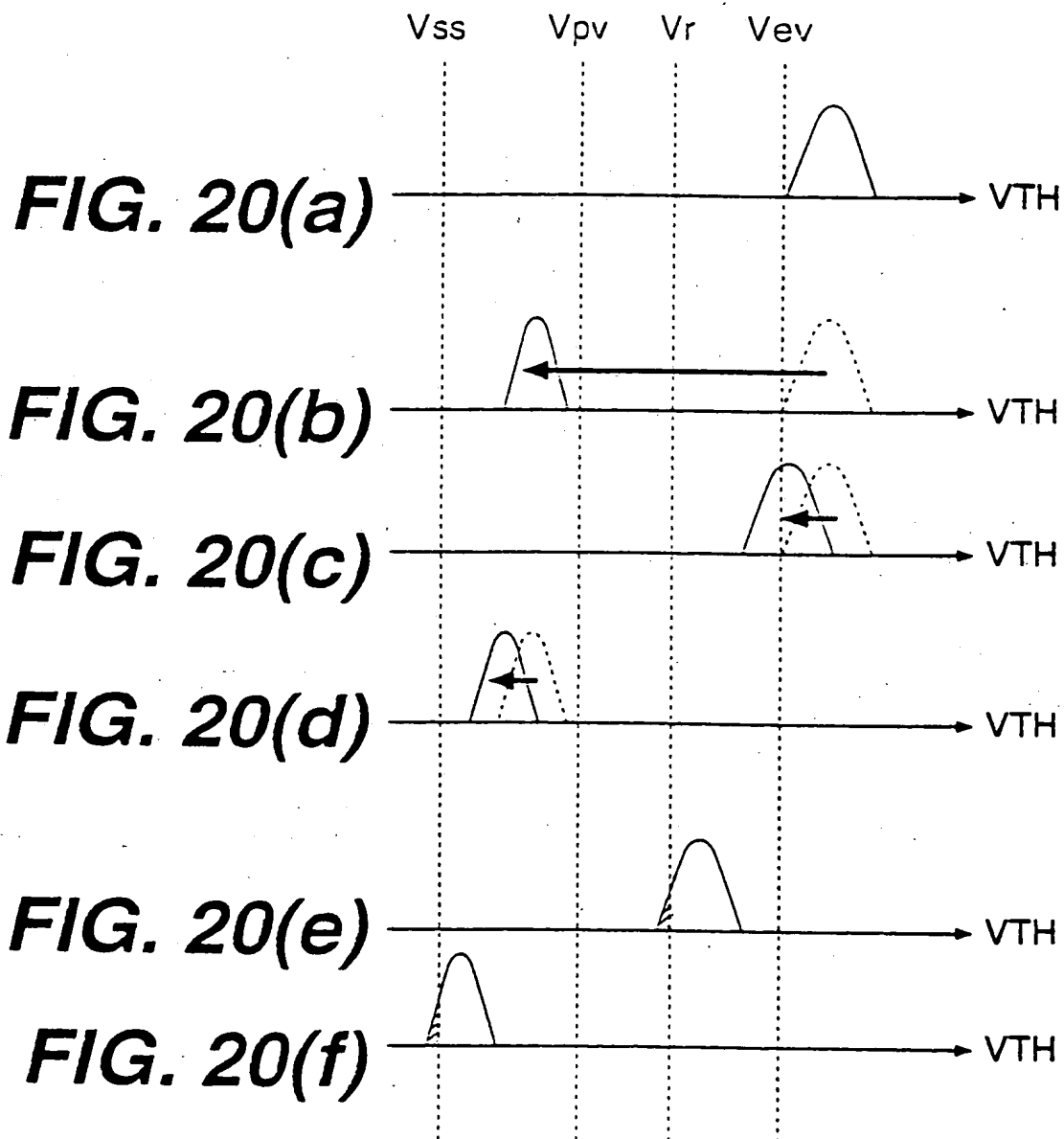


FIG. 19

PRIOR ART



PRIOR ART

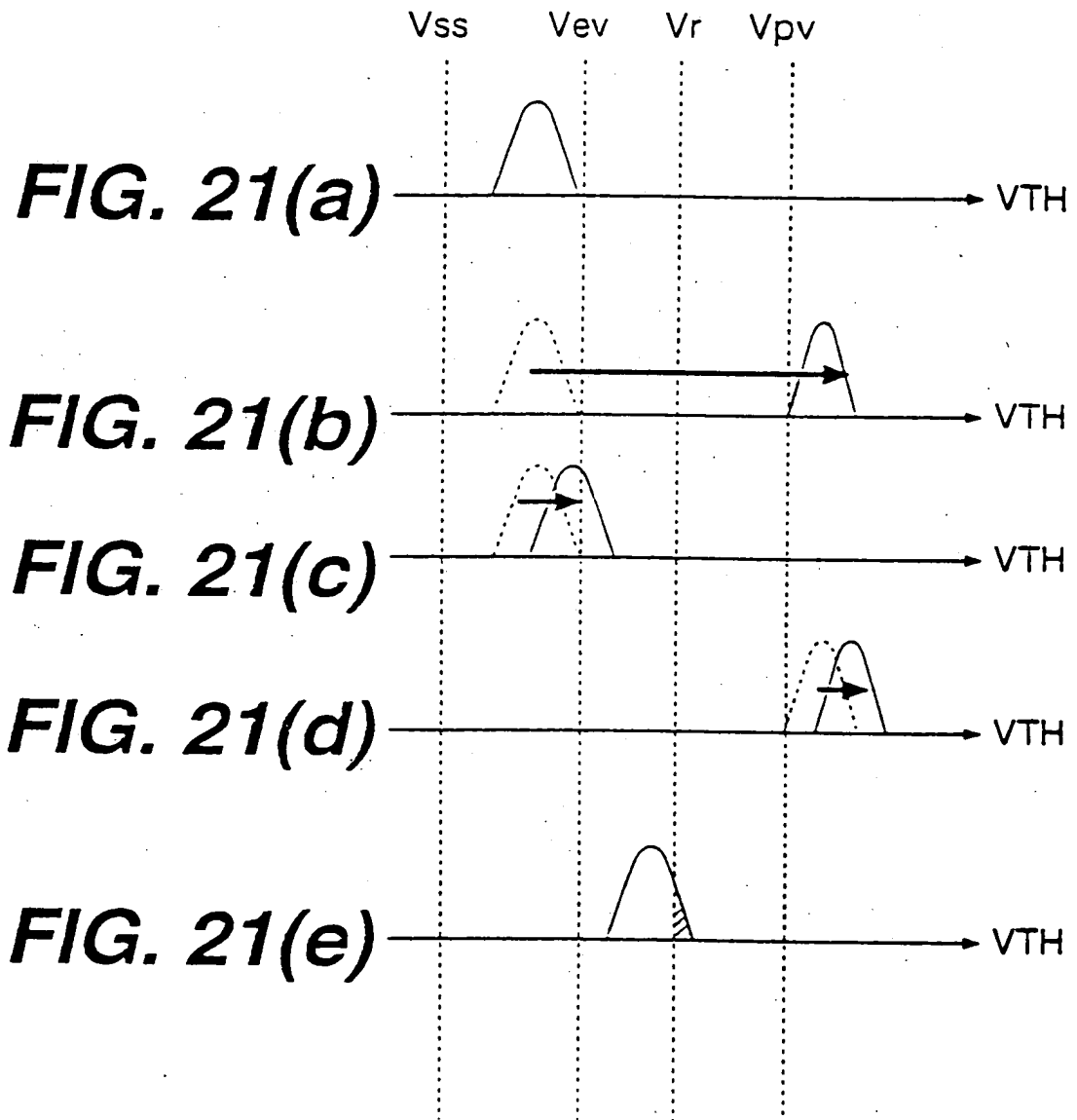


FIG. 22(a)

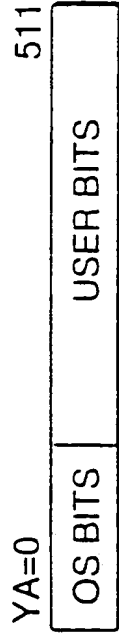
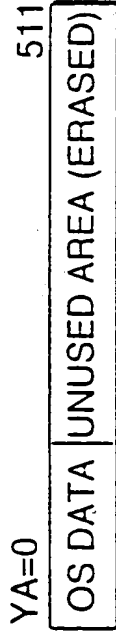


FIG. 22(b)



ADDITIONAL WRITE
↓

FIG. 22(c)

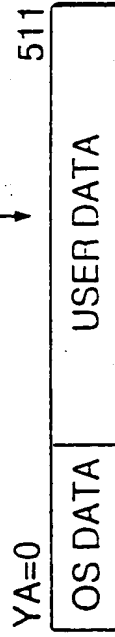


FIG. 22(d)

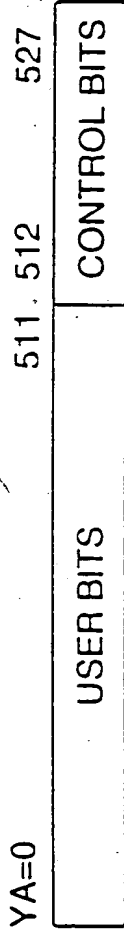


FIG. 22(e)



ADDITIONAL WRITE
↓

FIG. 22(f)



SECOND
STATE
(WRITTEN
STATE,
LOGICAL
STATE '0')

FIRST STATE
(ERASED
STATE,
LOGICAL
STATE '1')

V_{ss}

V_{pv}

V_r

V_{ev}

FIG. 23(a)

V_{TH}

FIG. 23(b)

V_{TH}

FIG. 23(c)

V_{TH}

FIG. 23(d)

V_{TH}

FIG. 23(e)

V_{TH}

FIG. 23(f)

V_{TH}

